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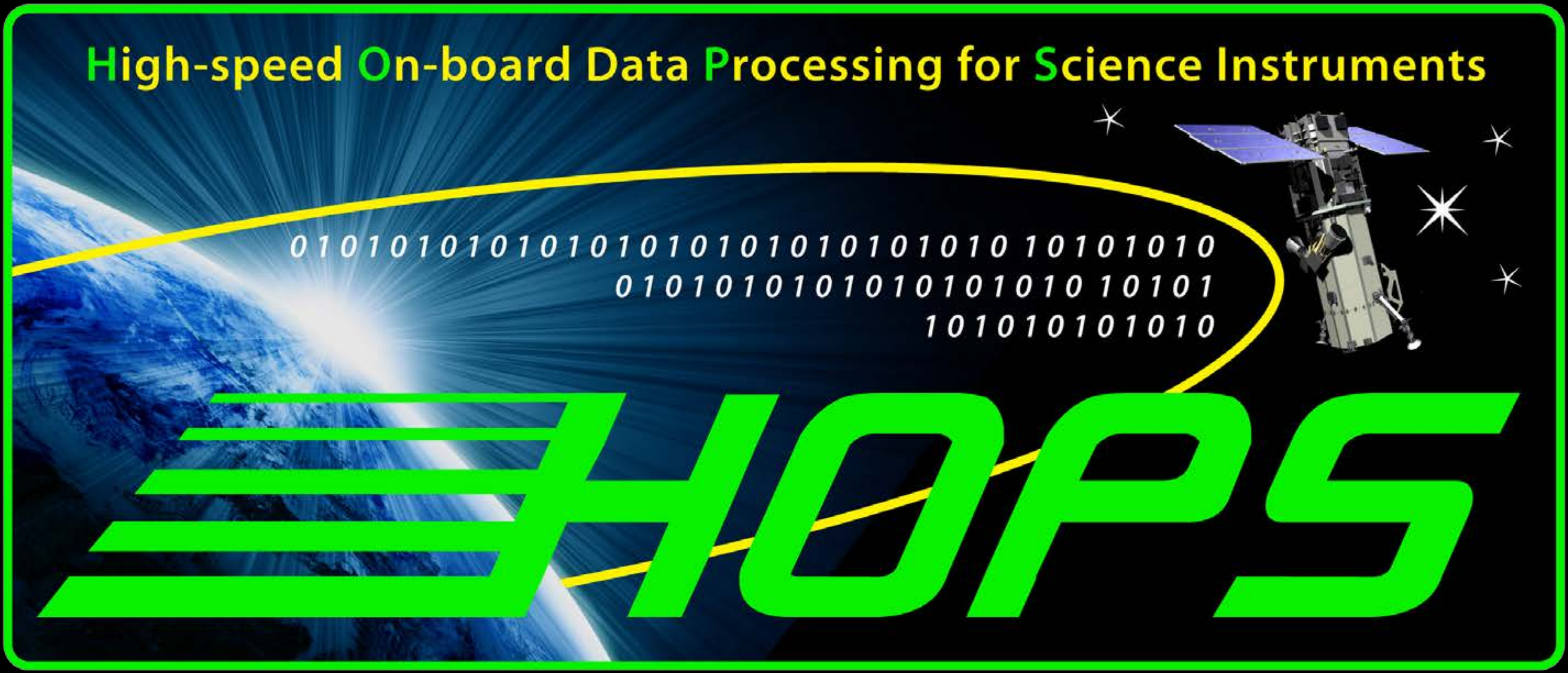

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December 18, 2015

LaRC

High-Speed On-Board Data Processing Platform for LIDAR Projects at NASA Langley Research Center

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Earth Science Technology Office

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Outline

- Introduction
- Accomplishments
- Approach
- Key Milestone History
- Integration of HOPS into Science Projects
- HOPS – Concept to Flight
- HOPS Collaboration
- Key Contributors
- Acknowledgment and Q&A

Earth Science Technology Office

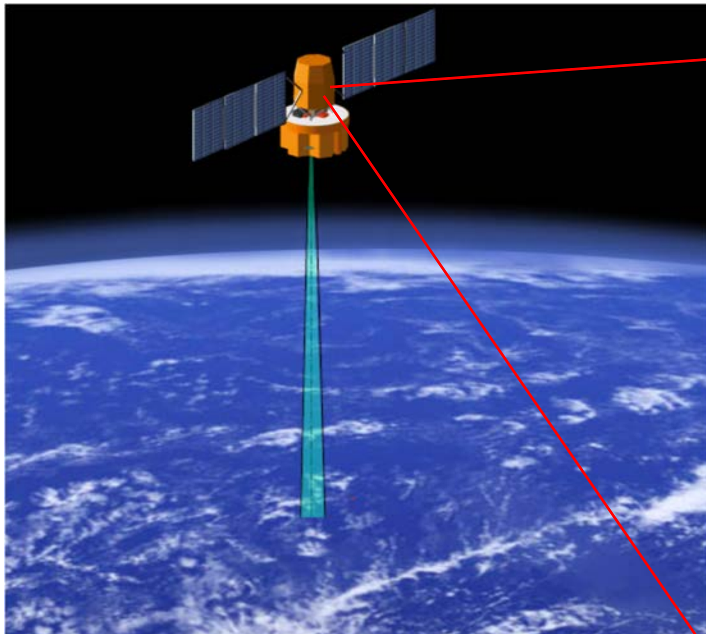
Introduction

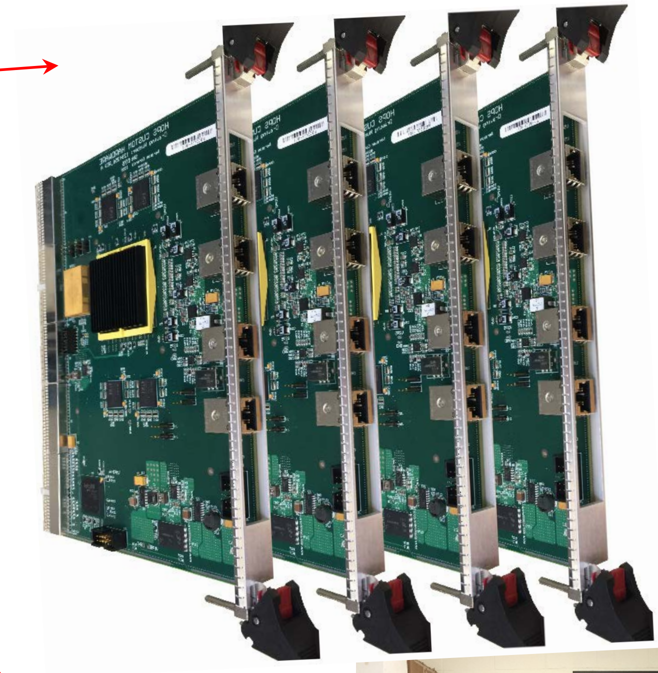
- Funded by NASA's ESTO (Earth Science Technology Office) AIST (Advanced Information Systems Technology) program.
- Period: April, 2012 – April, 2015
- Entry TRL 2, Exit TRL 5.
- Goals
  - Develop a high-speed, on-board reconfigurable and scalable data processing platform for science instruments
  - Demonstrate HOPS capabilities to address computationally intensive ASCENDS and 3-D Winds algorithms.
    - ASCENDS: Active Sensing of CO2 Emissions over Nights, Days, and Seasons
  - Demonstrate HOPS is reconfigurable and scalable.

Accomplishments

- HOPS Hardware (HW) offers high performance, scalable and re-configurable real-time data processing capabilities to high data volume missions.
- 6U HOPS HW offers 20 GB/sec of FPGA-memory bandwidth and 4 GB/sec of inter-board bandwidth.
- HOPS HW is path-to-flight while reducing the risk in the transition to TRL 6.
- HOPS HW reduces the power and mass by more than one order of magnitude than SOA radiation tolerant hardware.
- HOPS HW costs $20K, and its flight radiation tolerant HOPS cost estimate is 1-2 orders of magnitude less than SOA radiation tolerant hardware for equivalent processing capacity.
- HOPS HW prototype using COTS successfully completed two flight campaigns on the HU25B and the DC-8 demonstrating the real-time on-board processing capabilities. Such an end-to-end demonstration is equivalent to the demonstration of HOPS HW.
- HOPS HW enables ASCENDS and 3-D Winds to perform real-time on-board data processing while reducing the data volume up to 99%. HOPS HW is 30 to 700 times faster in 64K FFT computing than SOA radiation tolerant hardware.

Accomplishments





On-board processing enabling real-time processing

Reduced downlink data volume and terrestrial data processing time

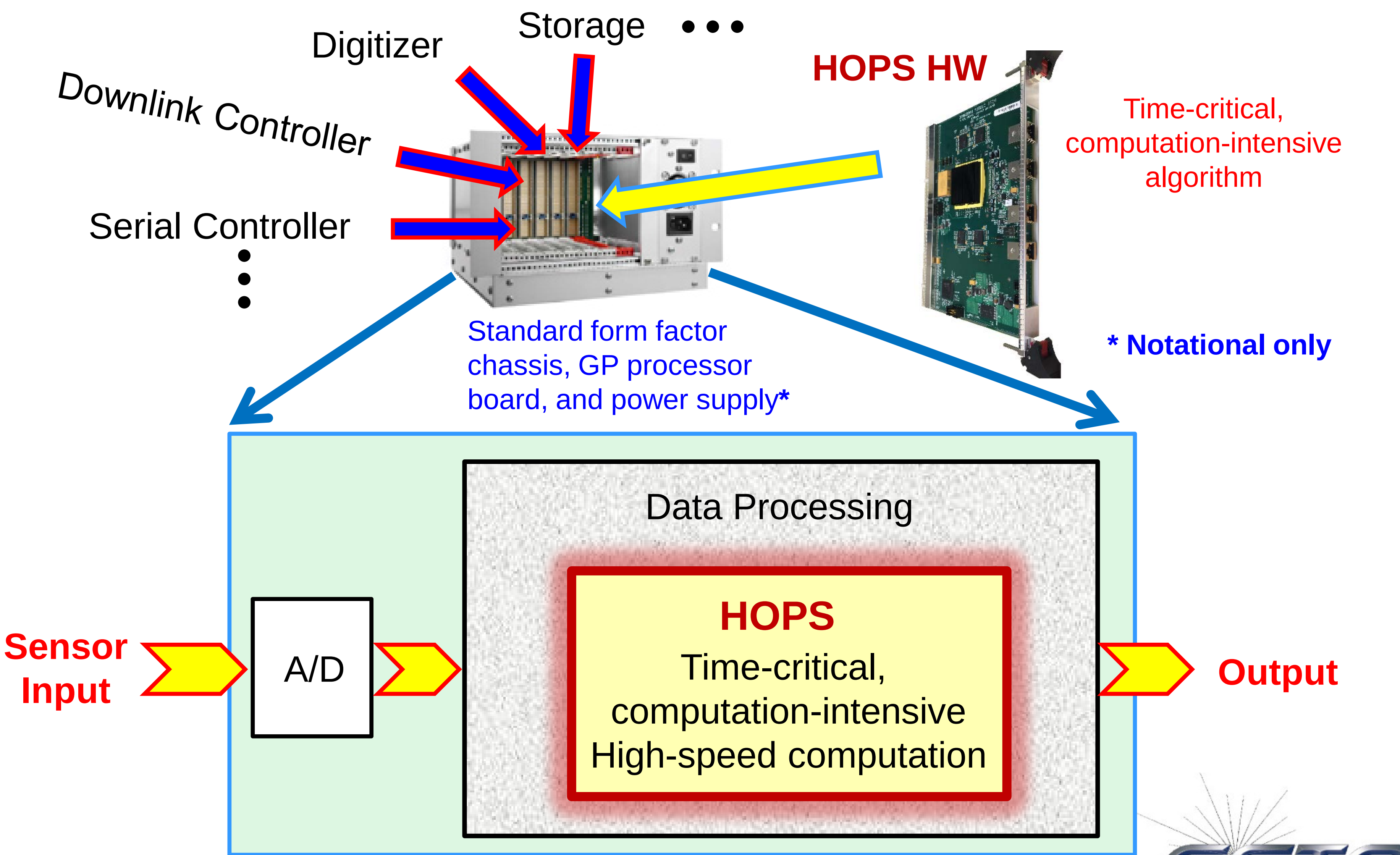
Approach

- Select representative algorithms for requirement definition and demonstration.
- Develop a software-based HOPS model that simulates timing, functions, and data volume accurately.
- Develop a HOPS prototype using COTS products and verify timing and functionality.
- Develop the final HOPS hardware derived from the software-based model and the COTS prototype.
- Demonstrate selected algorithms.

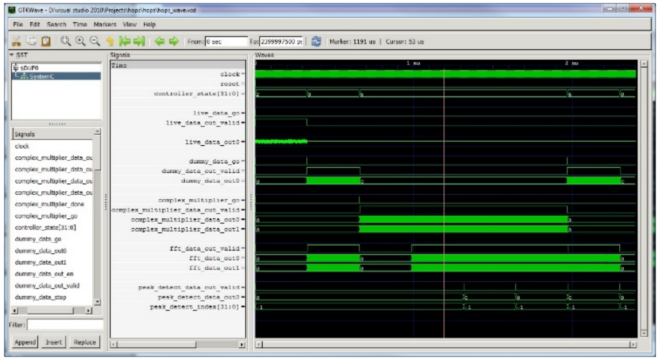
Key Milestone History

Key Milestones	Date
Define high-speed computing architecture and model.	09/2012
Demonstrate algorithms on software-based HOPS model.	03/2013
Prototype HOPS with COTS hardware. Develop VHDL for algorithm.	09/2013
Test algorithm on COTS hardware and architecture refinement.	12/2013
Design and build HOPS hardware. VHDL porting.	03/2015
Test, verify data processing algorithms on HOPS hardware.	04/2015

Integration of HOPS into Science Projects

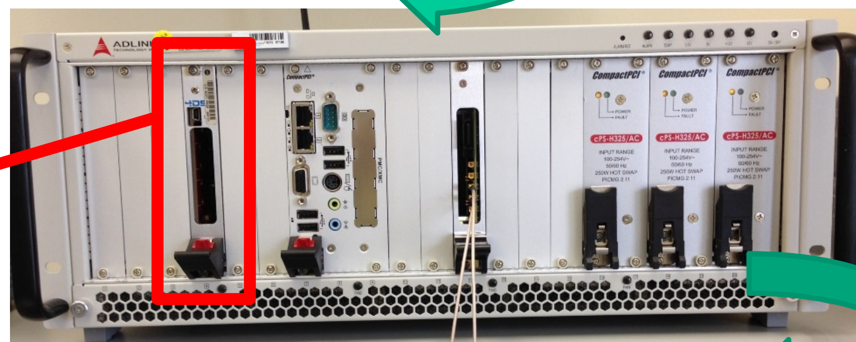


HOPS – Concept to Flight



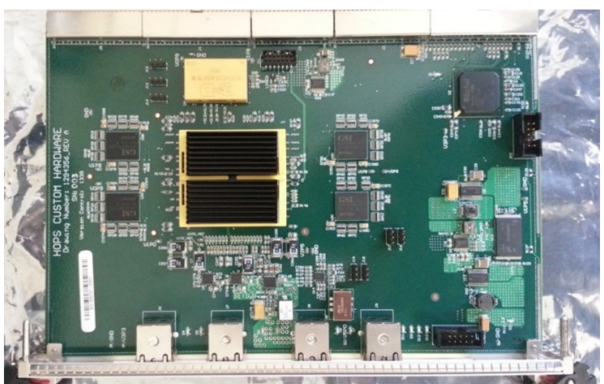
SystemC

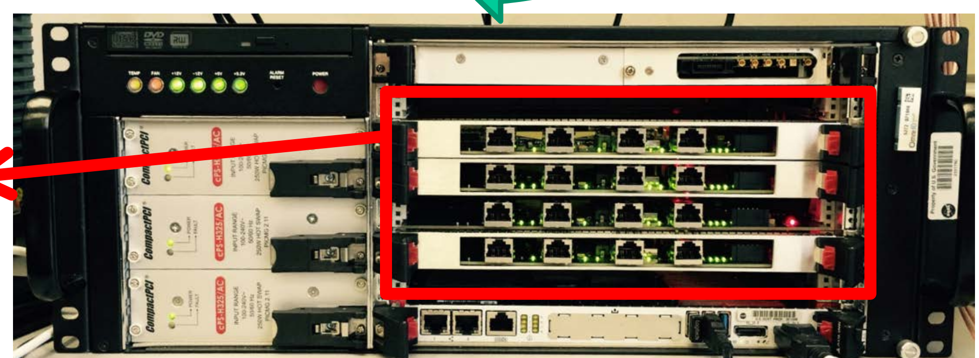
HOPS COTS (3U)



HOPS HW (6U)

(Superset of HOPS COTS in operations and functionalities)





HOPS Collaboration

- LaRC science teams: ACES, ASCENDS, and DAWN (3-D Wind)
- LaRC Engineering Directorate branches: Thermal and Mechanical
- Other NASA centers and contractors
  - Armstrong Flight Research Center (AFRC): HOPS COTS integration in the DC-8.
  - Exelis Inc. HOPS COTS flight demonstration with MFLL instrument.
  - Kennedy Space Center (KSC): Joint proposal effort discussion
- Academia
  - University of Florida (UF) in Gainesville: NSF CHREC (Center for High-Performance Reconfigurable Computing)
  - University of Michigan (UM) in Ann Arbor
  - Summer intern students: 1 in 2013 and 3 in 2014 (UF and UM)

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HOPS Collaboration

Summer Students.

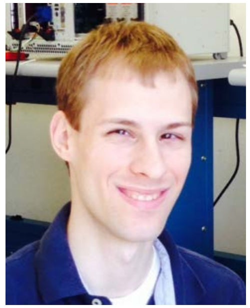
From left to right:

Dorothy Wong (U of FL – Gainesville)
Aaron Crasner (U of MI – Ann Arbor)
Kazumitsu Onishi (U of FL – Gainesville)

Earth Science Technology Office

Key Contributors (in random order)

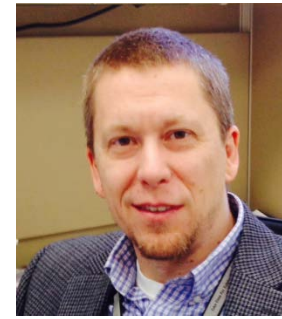
Dr. Tak Ng
Co-I. FPGA.
HOPS Architecture.



Jordan Davis
Board Design.
Flight Op. IT.
HU-25 & DC-8.

James Adams
PCB Design.
PRs. HU-25 &
DC-8.

Mark Hutchinson
Branch Head. HOPS
Signal Conditioning
for DC-8. Resources.
Staffing.



Kevin Somerville
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Board Design.

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Conditioning
for DC-8.

Charles Antill
HOPS Signal
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Jim Fay
Flight Op. IT.
DC-8.

Dr. Michael Obland
PI for ACES.
HU-25.

Byron Meadows
PM for ASCENDS.
DC-8.

Acknowledgments

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NASA SMD Earth Science Technology Office (ESTO),

and the ESTO Advanced Information System Technology

(AIST) program.

Acronym List

- ACES: ASCENDS CarbonHawk Experiment Simulator
- AIST: Advanced Information Systems Technology
- ASCENDS: Active Sensing of CO2 Emissions over Nights, Days, and Seasons
- CHREC: Center for High-Performance Reconfigurable Computing
- COTS: Commercially Off The Shelf
- ESTO: Earth Science Technology Office
- FPGA: Field-Programmable Gate Array
- GP: General Purpose
- HOPS: High-Speed On-Board Data Processing for Science Instruments
- HOPS HW: HOPS Hardware. aka HOPS custom board. Final deliverable.
- IT: Integration and Testing
- MFLL: Multifunctional Fiber Laser Lidar
- PI: Principal Investigator
- PM: Project Manager
- TRL: Technical Readiness Level
- UF: University of Florida
- UM: University of Michigan
- VHDL: VHSIC Hardware Description Language